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REVIEW OF BACK CONTACT SILICON SOLAR CELLS FOR LOW COST APPLICATION

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ABSTRACT: This paper will review back-contact silicon solar cell technologies for low-cost applications. Back contact solar cells have the advantages of zero or reduced grid shading and simplified module assembly. As silicon material costs decrease, module assembly will become a significant aspect of overall module costs. There are three design categories of back contact cells, the Interdigitated Back-Contact (IBC) solar cell, the Emitter Wrap-Through (EWT) solar cell, and the contact wrap-through solar cell. Each cell design is currently under investigation for low-cost application. The recent development of a 15.3 % efficient, 41 cm^2 EWT solar cell with screen-printed contacts is discussed. High-throughput and low-cost processing are the current research issues in each cell design.
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1. MOTIVATION

Back contact solar cells hold significant promise for increased performance in photovoltaics for the near future. The two major advantages that these cells possess are a lack of grid shading loss and co-planar interconnection. Front contacted cells can have up to 10 % shading loss when using screen printed metal grids. A front contact cell must also use solder connections that run from the front of one cell to the back of the next for series interconnection. This procedure is more difficult to automate than when using co-planar contacts.

The challenge is to produce a high efficiency cell at low cost using high throughput techniques. This has yet to be achieved with a back contact cell design. The focus of this paper will be to review the relevant features of back contact cells and progress made toward the goal of a low cost version of this device.

All of the back contact cells developed to date fall into three categories, which can be referred to as the Interdigitated Back Contact (IBC) cell, the Emitter Wrap-Through (EWT) cell and the contact wrap-through cell. IBC includes all of those cell designs with back contacts that rely upon carrier collection at a rear surface alone. The EWT class of cells can accomplish carrier collection at both sides and relies upon current conduction from the front to the back through some sort of perforation in the cell. The contact wrap-through cell maintains a front contact grid and brings the busbar or its equivalent to the back side through a minimum number of perforations.

2. IBC CELL

The IBC cell must be fabricated on material with a long minority carrier diffusion length. The distance from any point in the cell to the junction must be much less than the diffusion length. Excellent front surface passivation is required as well.

The IBC cell has the advantage of allowing the rear junction to be optimized for electrical performance, namely a low J_0 junction [1]. There is no need to conduct current along a diffused emitter, as is the case with a front contact cell. Hence, the tradeoff between series resistance and grid shading is not present in this design.

The IBC cell has been around since the 1970's, and is a very well developed technology. SunPower Corp. and Amonix have been commercializing these cells for several years. The cells are very high efficiency and are marketed for specialized applications. There has been little work in attempting to convert this device design into a low cost competitor in today's one sun flat plate market.

In the classical IBC cell, there are several photolithography steps for defining the emitter, back surface field, contact cuts, and metal gridlines. One simplified approach to IBC cell fabrication has been developed by Sinton[1], referred to as the trench mesa design. This process has demonstrated very high cell efficiencies (~22 % for moderate areas of 10.5 cm^2). This process uses one photolithography step to create steps and interdigitated P+ and N+ diffusions at the back. A full area metal deposition on the back side gives a natural isolation of p and n contacts due to absence of step coverage by the deposited metal. This process is very attractive since it requires no alignments at all, however it is dependent on the properties of a vacuum deposited metal. Vacuum deposition is generally not viewed as a low-cost process. Also, contact coverage is not selective, and contacts are a major recombination source.

It is possible to combine emitter formation and contacting into one step by the use of self-doping metallizations. This idea has been proposed previously by Meier [2]. The self-doping metal concept uses a metal/dopant compound applied to the silicon. This is followed by a high temperature step above the metal-silicon eutectic temperature to form an epitaxial silicon junction or back surface field by liquid phase growth. The metal remains to form a contact to the grown layer. This concept has the advantage of reducing process steps and producing a contact that is self-aligned to the junction. The process would require two applications of different self-doping metal compounds and one high temperature cycle. The second metal would need to be aligned to the first metal gridline pattern. A 10.4 % efficient cell was reported using aluminum as the p-contact and antimony-doped silver as the n-contact [2].

One drawback to the self-doping metal approach is that the junction area, and hence, metal coverage fractions, are high on the back surface. This adversely affects light trapping by reducing back surface reflectivity. Additionally, contact recombination is higher when compared to a selective contact. However, it is important to note that minimizing contact recombination requires a thick emitter of moderately high doping under the contact. In conventional emitter formation techniques, this requires

a very long high-temperature solid state diffusion. However, thick epitaxial layers can be grown in much shorter time.

Perhaps the main advantage of the self-doping metal concept is the ability to getter the silicon during processing by segregation of impurities to the molten metal contacts. Material quality necessary for an IBC cell structure is still marginal in most industrial silicon materials, and hence, the gettering may turn out to be a decisive advantage.

A fine n-type gridline is typical for an IBC cell fabricated on n-type material due to the two-dimensional collection present in this cell design. More specifically, the p-type junction fingers cannot be separated by more than a minority carrier diffusion length. However, a study by Ghannam, et.al. concludes that gridline tolerances needed for an efficient IBC cell are within the technological capability of screen printing [3]. This study, however, predicted superior performance by a front contacted cell in comparison to the IBC cell with typical material quality and cell thickness available in industrial silicon materials at present. The primary limitation is developing high quality silicon materials and overcoming handling issues with very thin cells.

The IBC cell is most easy to implement on rectangular substrates of limited width. Grid lines must be limited in length before causing series resistance problems and hence must run parallel to the short edge. Rectangular substrates are a natural feature of many thin ribbon silicon materials.

The IBC cell design should receive reconsideration in the near future as ribbon silicon growth techniques, which are well adapted to thin wafer production, become more prominent. The IBC design will only make an impact on the one sun solar cell market assuming that the issues of wafer thickness, material quality and process simplifications are successfully addressed. Uniformity of material will also be a significant issue, since lifetime variation in the IBC cell design can dramatically effect cell yield.

3. CONTACT WRAP THROUGH CELLS

The contact wrap-through has a front junction and front grid metal with the busbar or contact pads brought to the back through a small number of holes. This design is a compromise between an all back-contact cell and a conventional front contact cell in that it maintains the interconnection benefits but does not eliminate grid shading. A recent demonstration of this device was accomplished using merely 12 holes on a 100 cm^2 solar cell [4].

Another implementation of this structure recently under renewed development by ECN is the Pin-Up Module[5]. This is a conventional front emitter solar cell with a small number of holes. The front gridlines conduct current toward the holes where a small pin added during module assembly brings the contact to the back. The primary advantage is simplification in module assembly. Front grid shading is only slightly less than with a conventional front contact cell, but series resistance does not increase with larger area wafers due to the subdivision of current at each hole. In addition, the process appears compatible with current cell fabrication processes with the exception of the holes. This design is perhaps the least different from the conventional solar cell process and hence, could be implemented the most easily of back contact configurations.

4. EMITTER WRAP-THROUGH CELL

The EWT cell is well suited to lower quality silicon materials owing to its ability to collect carriers from both sides. The device does not require close grid spacing since carrier collection is nearly one-dimensional. There have been numerous design variations in recent years.

The buried contact EWT cell was one of the earliest versions developed [6]. It used laser drilled holes as well as laser cut channels for contact plating. The advantage to this structure was the economy of laser use. This design variation suffered from processing difficulties. The highest efficiency obtained was 8.8 % on a 36 cm^2 cell.

Recent efforts have focused on developing an EWT cell using screen printing technology [7]. The research group at ECN is fabricating 100 cm^2 cells using screen printing for all patterning steps. Holes are drilled by laser in the usual fashion. The process sequence involves an n-type diffusion over the entire wafer surface following hole drilling and damage etch. The n-type emitter is chemically etched on a portion of the back surface after the remaining surface is protected with an etch resist print. Metal contacts are applied by screen printing in two successive print and fire steps. The best cell reported was 9.6 % on 102 cm^2 using multicrystalline silicon. Poor passivation of the p-type surface was suggested as the limiting factor in cell efficiency [7]. The processes used in this cell fabrication sequence are all compatible with current industrial solar cell practices with the exception of the laser drilling.

A variant on the EWT cell concept is based on the POWER cell. The acronym stands for Polycrystalline Wafer Engineering Result. This cell forms the holes in the silicon by perpendicular dicing grooves--one on the cell front and one on the cell back. The groove depth is slightly deeper than half of the wafer thickness, and the hole diameter is controlled by the cut depths. The cell design has some unique advantages. First, light trapping can be obtained on polycrystalline silicon, due to the grooves. Collection efficiency can potentially be very high on poor quality silicon, due to a short distance of any point in the cell to a collecting junction. Also, the holes are formed in parallel with high throughput. Device results on a related cell structure using laser drilled holes were recently presented, with a 12.2 % efficient cell on CZ silicon [8].

The most successful EWT device to date in terms of cell efficiency has been based on photolithography patterning developed at Sandia. An emitter diffusion was masked by a deposited oxide and contacts applied using evaporated metal. The intention was to demonstrate a device design with a minimum of complications by the use of well-developed process techniques. An 18 % cell of 41 cm^2 area was recently reported[9]. The base material was 0.4 Ohm-cm silicon with a bulk lifetime of approximately 7 µsec, which demonstrates the potential of this device on low quality material. This is the highest efficiency reported for any EWT-type cell.

The photolithography-based EWT cell developed at Sandia has never suffered from the soft-knee diode

characteristic often observed in other EWT cell designs. This is attributed to the use of oxide passivated surfaces at the back of the cell. This surface is more sensitive than the surfaces of a conventional front-contact, front-junction cell due to the large junction perimeter intersecting the back surface of the EWT. A fill factor limitation that was observed in the photolithography-based cell was due to a localized region of high series resistance at the edges[9]. However, this was a linear effect in voltage present only in the illuminated solar cell. Diode characteristics are essentially ideal after elimination of the edge effects. The soft-knee diode characteristics present in other EWT cell designs have been attributed to inadequate surface passivation[10]. A surface passivation for the EWT cell must minimize surface recombination as well as surface conductance channels. This rules out bare silicon surfaces and high charge density dielectrics, such a deposited silicon nitride, for back surface passivation of the EWT. A thermal oxide or densified deposited oxide are the ideal materials to passivate the back surface of the EWT cell.

5. RECENT EWT RESULTS

Sandia has recently demonstrated an EWT cell using screen printed contacts. A 41 cm^2 cell with 15.3 % efficiency under AM1.5G illumination was achieved. Several other cells had similar efficiencies. Screen printed aluminum formed the p-contact and screen printed silver was used for the n-contact. Emitter patterning was done by photolithography of a deposited mask oxide. Emitter line widths were quite large at 0.8 mm. This large line width holds open the possibility of alternative patterning techniques that can avoid photolithography.

5.1 Cell process

The first step in EWT fabrication is deposition of a CVD mask oxide on the back of the cell. This mask oxide is typically borosilicate glass capped with un-doped SiO_2. Holes are drilled from the back side with a Nd-YAG laser. A damage removal etch in KOH is followed by photolithographic patterning of the mask oxide. This is followed by a crystallographic texture etch and a phosphorous diffusion. Screen-printed contacts are applied directly to the oxidized surfaces after phosphorous diffusion. DuPont 4943 silver paste was used for the n-contact and either aluminum or silver/aluminum paste used for the p-contact. Contacts were co-fired in a belt furnace at approximately 730 C.

In early versions of the screen-printed cell, shunt conductance was high and cell blue response was much worse than evaporated contact controls. These cells were surface passivated by a thin thermal oxide. The shunting was consistent from cell to cell and was also present in small test diodes which did not possess holes. The shunt conductance was attributed to contact spiking through the junction. The poor blue response was a result of contamination in the belt furnace. Both process problems were solved by retaining the thick oxides on the cell surfaces, approximately 100 nm on the n-type surface resulting from the phosphorous diffusion and approximately 300 nm of mask oxide on the p-type surface. The thick oxides alleviated shunting problems as well as acting as diffusion barriers to impurities in the firing process.

5.2 Device Results

The I-V curve under AM1.5G illumination for the 15.3 % efficient EWT cell is shown in Figure 1. The cell is approximately 280 μm thick, 41 cm^2 area, on 0.5 Ohm-cm c-Si. The emitter sheet resistance is 45 Ohm/square. Contact coverage on the back of the cell is 40 %. Fraction of p-type area on the back surface is 40 %.

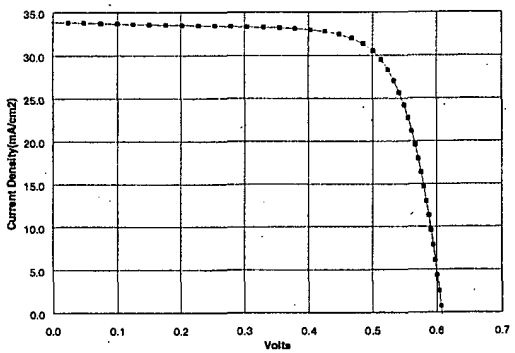

Figure 1. I-V curve under AM1.5G illumination for EWT cell with screen printed contacts

The largest fill factor loss for this EWT cell is series resistance, contributing about 5.5% power loss, with non-ideal diode recombination contributing about 4.5 % power loss. Shunt conductance is the smallest contributor giving only a 1.5 % loss. Series resistance is approximately 0.9 Ohm-cm^2 and is dominated by contact resistance and the resistance of the holes.

Recombination losses are dominated by bulk recombination in the base. Lifetimes typical of the material used were 5-10 μsec as measured by RF-PCD on control samples passivated by a light N+ diffusion. Quantum efficiency and reflectance data of the 15.3 % efficient cell are shown in Figure 2.

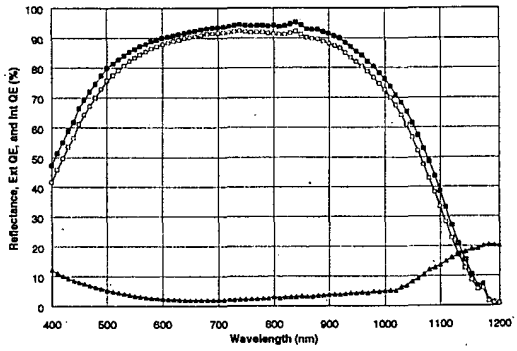

Figure 2. Internal, External Quantum efficiency and reflectance of 15.3 % efficient screen printed EWT solar cell.

5.3 Future work, EWT

There are many opportunities to improve the EWT cell. The EWT has had the disadvantage of comparison with the proven IBC cell design. The efficiency potential of the EWT has been slow to appear because most research has used industrial techniques from the start. It is difficult to accept a cell design which requires new processing techniques and has not shown high efficiencies. The IBC cell has demonstrated among the

highest efficiencies measured for c-Si solar cells, but the design is sensitive to low lifetimes. The EWT cell is much better adapted to simple processing techniques since grid line spacing can be very relaxed, and poor quality material can be tolerated with less decline in efficiency than either the front-contact cell or the IBC cell. Cell yield will become an increasing concern for manufacturing processes, and the EWT is less susceptible to lifetime-related yield problems.

A primary technical challenge for higher efficiency in the EWT cell is getting metal in the holes to minimize series resistance. Also, the cell would benefit from a selective emitter even more than a front contact cell due to the large junction area in the EWT. For processing lower quality materials, a gettering step is always helpful. All three of these features could be incorporated by the use of self-doping contacts mentioned previously.

The EWT cell is well adapted to relatively thick silicon materials of low and variable quality. These characteristics are most often found in multicrystalline silicon cut from ingots. The EWT cell could most benefit this class of materials. Throughput concerns over laser drilling could be alleviated by drilling holes through entire ingots.

The EWT cell has only recently demonstrated high efficiency potential. Future work should center around adapting the cell design to high-throughput processes. Most effort will need to focus on the emitter formation step.

6. CONCLUSIONS

As silicon material costs continue to decline, module assembly will begin to dominate total costs for one-sun, c-Si modules. Back contact solar cells have the potential to alleviate these assembly costs due to co-planar contacts. Several device options exist for back-contact cells. The design closest to implementation is the contact wrap-through design class, since it is the least radical departure from current technology. However, these cells do not have the efficiency potential of other back contact cell designs.

The IBC cell has demonstrated efficiency potential and many favorable device characteristics. However, it is a very demanding cell structure to implement. Advances in handling thin silicon materials, increased material quality and uniformity, as well as novel contact technologies will be required for the a low-cost, high-throughput version of this cell design. It is best adapted to thin ribbon silicon materials.

The EWT cell is less sensitive to material quality fluctuations, and can be made without fine gridlines and tight tolerances. It is well adapted lower quality, variable silicon materials, and can reduce cell yield loss from lifetime fluctuations.

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